Listing of Claims:

This Listing of Claims will replace all prior versions and listing of claims in the Application.

1. (Previously Amended) A circuit for reducing clock signal skew comprising:

at least a first and second complementary clock signal input/output line for receiving first and second complementary clock input signals and transmitting first and second complementary clock output signals, wherein the complementary clock input signals have a skewed time lag relative to each other;

first and second inverters each having an input and an output, said input of said first inverter connected to said output of said second inverter and to said first clock signal input/output line and said input of said second inverter connected to said output of said first inverter and to said second clock signal input/output line, wherein the first and second inverters function to reduce the skew present in the complementary clock input signals.

2. (Original) The circuit of claim 1 further comprising an enable circuit for receiving an enable signal and enabling or disabling said first and second inverters in response to the enable signals.

3. (Previously Amended) The circuit of claim 2, wherein said enable circuit comprises:

a first voltage source for supply of a first voltage to said first inverter and said second inverter, said first voltage supply being coupled to said inverters by the enable signal;

an enable inverter for inverting the enabling signal;

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a second voltage source for supplying a second voltage to said second inverter and said first inverter, said second voltage source being coupled to said first and second inverters by the inverted enable signal.

4. (Previously Amended) The circuit of claim 3, wherein said first voltage source is coupled by a P-channel transistor responsive to the enable signal.

5. (Previously Amended) The circuit of claim 3, wherein said second voltage source is coupled by a N-channel transistor responsive to the inverse of the enable signal.

6. (Previously Amended) The circuit of claim 3, wherein said first voltage source is coupled by an N-channel transistor responsive to the enable signal.

7. (Previously Amended) The circuit of claim 3, wherein said second voltage source is coupled by an P-channel transistor responsive to the inverse of the enable signal.

8. (Previously Amended) The circuit of claim 1, further comprising first and second input buffer circuits for receiving first and second external complementary clock signals and respectively supplying said external complementary clock signals to said first and second complementary clock signal input/output line.

9. (Previously Amended) The circuit of claim 8, wherein each of said first and second input buffer circuits comprises:

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an input for receiving one of said first and second external complementary clock signals;

an input for receiving a reference voltage signal;

a differential amplifier coupled to said inputs, said differential amplifier having an output terminal for providing a latch signal in response to the external clock signal in comparison to the reference voltage signal, the latch signal having a first or second state;

a buffer circuit inverter connected to said output terminal of said differential amplifier, said buffer circuit inverter generating a first internal clock signal when the latch signal is in a first state, and a second, complementary internal clock signal when the latch signal is in a second state; and

an input line for transmitting said first or second internal clock signal, said input line connected to one of said first and second complementary clock signal input/output lines.

10. (Original) The circuit of claim 9, further comprising an enable circuit for receiving said enable signal and enabling or disabling said first and second input buffer circuits in response to the enable signal.

11. (Previously Amended) The circuit of claim 1, further comprising a first and second driver circuit, said first and second driver circuit connected to said first and second complementary clock signal input/output lines, respectively.

12. (Original) The circuit of claim 11, wherein at least one of said first and second driver circuits comprises at least a first and second driver inverter connected in series.

13. (Previously Amended) The circuit of claim 12, further comprising at least a third driver inverter connected in parallel to said first and second driver inverters, the output of said third driver inverter coupling the output of said first and second driver inverters to a predetermined voltage.

14. (Previously Amended) The circuit of claim 1, wherein each of said first and second inverters are comprised of series connected complimentary transistors, the respective connection terminal of said series connected complimentary transistors being coupled to a respective one of said complementary clock signal input/output lines.

15. (Previously Amended) The circuit of claim 14, wherein said first and second inverters include:

a first N-channel transistor coupled to a second N-channel transistor, a gate of said first N-channel transistor coupled to receive said second clock input signal, and said second N-channel transistor coupled to receive said first clock input signal;

a first P-channel transistor coupled to a second P-channel transistor, a gate of said first P-channel transistor coupled to receive said second clock input signal, and said second P-channel transistor coupled to receive said first clock input signal;

said second N-channel transistor coupled in series to said second P-channel transistor and said first clock signal input/output line connected between said second N-channel transistor and said second P-channel transistor; and

said first N-channel transistor coupled in series to said first P-channel transistor and said second clock signal input/output line connected between said first N-channel transistor and said first P-channel transistor.

16. (Previously Amended) A circuit for reducing clock signal skew comprising:

at least a first and second complementary clock signal input/output line for receiving first and second complementary clock input signals and transmitting first and

second internal complementary clock signals, wherein the at least first and second complementary clock signals have a time lag skew relative to each other;

a first N-channel transistor coupled to a second N-channel transistor, a gate of said first N-channel transistor coupled to receive said second clock input signal, and said second N-channel transistor coupled to receive said first clock input signal;

a first P-channel transistor coupled to a second P-channel transistor, a gate of said first P-channel transistor coupled to receive said second clock input signal, and said second P-channel transistor coupled to receive said first clock input signal;

said second N-channel transistor coupled in series to said second P-channel transistor and said first clock signal input/output line connected between said second N-channel transistor and said second P-channel transistor; and

said first N-channel transistor coupled in series to said first P-channel transistor and said second clock signal input/output line connected between said first N-channel transistor and said first P-channel transistor, wherein the transistors operate to output the at least first and second complementary clock signals with a reduced skew.

17. (Original) The circuit of claim 16, further comprising an enable circuit for receiving an enable signal and enabling or disabling said first and second N-channel transistors and said first and second P-channel transistors in response to the enable signal.

18. (Original) The circuit of claim 17, wherein said enable circuit comprises:

a third P-channel transistor having a source coupled to a voltage supply, a gate coupled to receive the enable signal, and a drain coupled to a source of said first and second P-channel transistors;

an enable inverter for inverting the enable signal; and

a third N-channel transistor having a drain coupled to a ground, a gate coupled to receive the inverted enable signal, and a drain coupled to a drain of said first and second N-channel transistors.

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19. (Original) The circuit of claim 17, wherein said enable circuit comprises:

a third N-channel transistor having a source coupled to a voltage supply, a gate coupled to receive the enable signal, and a drain coupled to a source of said first and second N-channel transistors;

an enable inverter for inverting the enable signal; and

a third P-channel transistor having a drain coupled to a ground, a gate coupled to receive the inverted enable signal, and a drain coupled to a drain of said first and second P-channel transistors.

20. (Previously Amended) The circuit of claim 16, further comprising first and second input buffer circuits for receiving first and second external complementary clock signals and respectively supplying said external complementary clock signals to said first and second complementary clock signal input/output line.

21. (Previously Amended) The circuit of claim 20, wherein each of said first and second input buffer circuits comprises:

an input for receiving one of said first and second external complementary clock signal;

an input for receiving a reference voltage signal;

a differential amplifier coupled to said input, said differential amplifier having an output terminal for providing a latch signal in response to the external clock signal in comparison to the reference voltage signal, the latch signal having a first or second state;

a buffer circuit inverter connected to said output terminal of said differential amplifier, said buffer circuit inverter generating a first internal clock signal when the latch signal is in a first state, and a second internal clock signal when the latch signal is in a second state; and

an input line for transmitting said first or second internal clock signal, said input line connected to one of said first and second complementary clock signal input/output lines.

22. (Original) The circuit of claim 21, further comprising an enable circuit for receiving said enable signal and enabling or disabling said first and second input buffer circuits in response to the enable signal.

23. (Previously Amended) The circuit of claim 16, further comprising a first and second driver circuit, said first and second driver circuit connected to said first and second complementary clock signal input/output lines, respectively.

24. (Original) The circuit of claim 23, wherein at least one of said first and second driver circuits comprises at least a first and second driver inverter connected in series.

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25. (Previously Amended) The circuit of claim 24, further comprising at least a third driver inverter connected in parallel to said first and second driver inverters, the output of said third driver inverter coupling the output of said first and second driver inverters to a predetermined voltage.

26. (Previously Amended) A circuit for reducing signal skew comprising:

at least a first and second complementary clock signal input/output line for receiving first and second complementary clock input signals and transmitting first and second complementary clock output signals, wherein the complementary clock input signals have a skewed time lag relative to each other;

first and second inverters each having an input and an output, said input of said first inverter connected to said output of said second inverter and to said first clock signal input/output line and said input of said second inverter connected to said output of said first inverter and to said second, complementary clock signal input/output line

wherein the first and second inverters operate to reduce the skew present in the complementary clock input signals; and a first and second driver circuit, said first and second driver circuit connected to said first and second clock signal input/output lines, respectively.

27. (Original) The circuit of claim 26, further comprising an enable circuit for receiving an enable signal and enabling or disabling said first and second inverters in response to the enable signal.

28. (Previously Amended) The circuit of claim 27, wherein said enable circuit comprises:

a first voltage source for supply of a first voltage to said first inverter and said second inverter, said first voltage supply being coupled to said inverters by the enable signal;

an enable inverter for inverting the enabling signal;

a second voltage source for supplying a second voltage to said second inverter and said first inverter, said second voltage source being coupled to said inverters by the inverted enable signal.

29. (Previously Amended) The circuit of claim 28, wherein said first voltage source is coupled by a P-channel transistor responsive to the enable signal.

30. (Previously Amended) The circuit of claim 28, wherein said second voltage source is coupled by a N-channel transistor responsive to the inverse of the enable signal.

31. (Previously Amended) The circuit of claim 28, wherein said first voltage source is coupled by an N-channel transistor responsive to the enable signal.

32. (Previously Amended) The circuit of claim 28, wherein said second voltage source is coupled by an P-channel transistor responsive to the inverse of the enable signal.

33. (Previously Amended) The circuit of claim 26, further comprising first and second input buffer circuits for receiving first and second external complementary clock signals and respectively supplying said external complementary clock signals to said first and second complementary clock signal input/output line.

34. (Previously Amended) The circuit of claim 33, wherein each of said first and second input buffer circuits comprises:

an input for receiving one of said first and second external complementary clock signal;

an input for receiving a reference voltage signal;

a differential amplifier coupled to said input, said differential amplifier having an output terminal for providing a latch signal in response to the external clock signal in comparison to the reference voltage signal, the latch signal having a first or second state;

a buffer circuit inverter connected to said output terminal of said differential amplifier, said buffer circuit inverter generating a first internal clock signal when the latch signal is in a first state, and a second internal clock signal when the latch signal is in a second state; and

an input line for transmitting said first or second internal clock signal, said input line connected to one of said first and second complementary clock signal input/output lines.

35. (Original) The circuit of claim 34, further comprising an enable circuit for receiving said enable signal and enabling or disabling said first and second input buffer circuits in response to the enable signal.

36. (Original) The circuit of claim 26, wherein at least one of said first and second driver circuits comprises at least a first and second driver inverter connected in series.

37. (Previously Amended) The circuit of claim 36, further comprising at least a third driver inverter connected in parallel to said first and second driver inverters, the

output of said third driver inverter coupling the output of said first and second driver inverters to a predetermined voltage.

38. (Previously Amended) A circuit for buffering a clock signal comprising:

a first and second input buffer circuit for receiving a first and second external clock signal, respectively, each of said input buffer circuits comprising:

an input for receiving one of said first and second external clock signals;

a differential amplifier coupled to the input, said differential amplifier having an output terminal for providing a latch signal in response to the external clock signal, the latch signal having a first or second state; and

a first inverter connected to said output terminal, said first inverter generating an internal clock signal in response to the latch signal, said first inverter generating a first internal clock signal when the latch signal is in a first state, and a second internal clock signal when the latch signal is in a second state; and

a circuit for reducing skew between the first and second internal clock signals, said circuit comprising:

first and second clock signal input/output lines for receiving and transmitting first and second internal clock signals, respectively; and

at least second and third inverters each having an input and an output, said input of said second inverter connected to said output of said third inverter and to said first clock signal input/output line and said input of said third inverter connected to said output of said second inverter and to said second clock signal input/output line.

39. (Original) The circuit of claim 38, further comprising an enable circuit for receiving an enable signal and enabling or disabling said first and second input buffer circuit and said second and third inverters in response to the enable signal.

40. (Previously Amended) The circuit of claim 39, wherein said enable circuit comprises:

a first voltage source for supply of a first voltage to said second inverter and said third inverter, said first voltage supply being coupled to said inverters by the enable signal;

an enable inverter for inverting the enabling signal;

a second voltage source for supplying a second voltage to said third inverter and said second inverter, said second voltage source being coupled to said inverters by the inverted enable signal.

41. (Previously Amended) The circuit of claim 40, wherein said first voltage source is coupled by a P-channel transistor responsive to the enable signal.

42. (Previously Amended) The circuit of claim 40, wherein said second voltage source is coupled by a N-channel transistor responsive to the inverse of the enable signal.

43. (Previously Amended) The circuit of claim 40, wherein said first voltage source is coupled by an N-channel transistor responsive to the enable signal.

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44. (Previously Amended) The circuit of claim 40, wherein said second voltage source is coupled by an P-channel transistor responsive to the inverse of the enable signal.

45. (Original) The circuit of claim 38, further comprising a first and second driver circuit for boosting said output signal, said first and second driver circuit connected to said first and second clock signal input/output lines, respectively.

46. (Original) The circuit of claim 45, wherein at least one of said first and second driver circuits comprises at least a first and second driver inverter connected in series.

47. (Previously Amended) The circuit of claim 46, further comprising at least a third driver inverter connected in parallel to said first and second driver inverters, the

output of said third driver inverter coupling the output of said first and second driver inverters to a predetermined voltage.

48. (Previously Amended) A circuit for buffering a clock signal comprising:

a first and second input buffer circuit for receiving a first and second external clock signal, respectively, each of said input buffer circuits comprising:

an input for receiving one of said first and second external clock signals;

a differential amplifier coupled to the input, said differential amplifier having an output terminal for providing a latch signal in response to the external clock signal, the latch signal having a first or second state; and

a first inverter connected to said output terminal, said first inverter generating an internal clock signal in response to the latch signal, said first inverter generating a first internal clock signal when the latch signal is in a first state, and a second internal clock signal when the latch signal is in a second state; and

a circuit for reducing skew between the first and second internal clock signals, said circuit comprising:

first and second clock signal input/output lines for receiving and transmitting first and second internal clock signals, respectively; and

at least second and third inverters each having an input and an output, said input of said second inverter connected to said output of said third inverter and to said first clock signal input/output line and said input of said third inverter connected to said output of said second inverter and to said second clock signal input/output line; and

a first and second driver circuit for boosting said output signal, said first and second driver circuit connected to said first and second clock signal input/output lines, respectively.

49. (Original) The circuit of claim 48, further comprising an enable circuit for receiving an enable signal and enabling or disabling said first and second input buffer circuit and said second and third inverters in response to the enable signal.

50. (Previously Amended) The circuit of claim 49, wherein said enable circuit comprises:

a first voltage source for supply of a first voltage to said second inverter and said third inverter, said first voltage supply being coupled to said inverters by the enable signal;

an enable inverter for inverting the enabling signal;

a second voltage source for supplying a second voltage to said third inverter and said second inverter, said second voltage source being coupled to said inverters by the inverted enable signal.

51. (Previously Amended) The circuit of claim 50, wherein said first voltage source is coupled by a P-channel transistor responsive to the enable signal.

52. (Previously Amended) The circuit of claim 50, wherein said second voltage source is coupled by a N-channel transistor responsive to the inverse of the enable signal.

53. (Previously Amended) The circuit of claim 50, wherein said first voltage source is coupled by an N-channel transistor responsive to the enable signal.

54. (Previously Amended) The circuit of claim 50, wherein said second voltage source is coupled by an P-channel transistor responsive to the inverse of the enable signal.

56. (Previously Amended) The circuit of claim 55, further comprising at least a third driver inverter connected in parallel to said first and second driver inverters, the output of said third driver inverter coupling the output of said first and second driver inverters to a predetermined voltage.

57-81. (Cancelled)

82. (Previously Amended) A method of generating an internal clock signal in an integrated circuit, the method comprising the steps of:

receiving first and second external clock signals, wherein the second external clock signal is an inverse of the first external clock signal and where there exists a time lag skew of one of said external clock signals relative to the other; and

modifying the transition of one of said external clock signals relative to the other to produce, from said external clock signals, internal clock signals which have reduced skew.

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83. (Original) The method of claim 82, further comprising the step of buffering each of the first and second external clock signals using a reference voltage.

84. (Original) The method of claim 83, wherein said step of modifying the transition of one of said buffered external clock signals comprises the step of transmitting each of said buffered external clock signals through series connected complimentary transistors, the respective connection terminal of said series connected complimentary transistors being coupled to respective input/output lines for receiving said first and second external clock signals.

85. (Original) The method of claim 83, wherein said step of modifying the transition of one of said buffered external clock signals comprises the steps of:

speeding the transition of said buffered external clock signal having a time lag; and

slowing the transition of the other of said buffered external clock signals.

86. (Original) The method of claim 82, further comprising the step of driving each of said internal clock signals.

87. (Previously Amended) The method of claim 82, wherein said act of receiving first and second external clock signals is performed in connection with the operation of a random access memory.

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88. (Original) The method as in claim 87, wherein said random access memory comprises a dynamic random access memory.

89. (Original) The method of claim 82, further comprising transmitting said internal clock signals to a memory circuit.

90. (Original) The method as in claim 89, wherein said memory circuit comprises a dynamic random access memory.

91. (Previously Amended) A method of generating an internal clock signal in an integrated circuit, the method of comprising the steps of:

receiving first and second external clock signals, wherein the second external clock signal is an inverse of the first external clock signal and where there exists a time lag skew of one of said external clock signals relative to the other;

buffering each of the first and second external clock signals using a reference voltage;

modifying the transition of one of said buffered external clock signals relative to the other to produce, from said buffered external clock signals, internal clock signals which have reduced skew.

92. (Original) The method of claim 91, wherein said step of modifying the transition of one of said buffered external clock signals comprises the steps of:

speeding the transition of said buffered external clock signal having a time lag; and

slowing the transition of the other of said buffered external clock signals.

93. (Original) The method of claim 91, wherein said step of modifying the transition of one of said buffered external clock signals comprises the step of transmitting each of said buffered external clock signals through series connected complimentary transistors, the respective connection terminal of said series connected complimentary transistors being coupled to respective input/output lines for receiving said first and second external clock signals.

94. (Original) The method of claim 91, further comprising the step of driving each of said internal clock signals.

95. (Original) The method of claim 91, wherein said act of receiving first and second external clock signals is performed in connection with the operation of a random access memory.

96. (Original) The method of claim 94, wherein said random access memory comprises a dynamic random access memory.

97. (Original) The method of claim 91, further comprising transmitting said internal clock signals to a memory circuit.

98. (Original) The method as in claim 96, wherein said memory circuit comprises a dynamic random access memory.